IN THE CLAIMS

Please amend the claims to the following.

1. (Currently Amended) An apparatus comprising:

a hardware managed stack to hold a plurality of VMX mask word values corresponding to a plurality of virtual machines (VMs), wherein a current VMX mask word value of the plurality of VMX mask word values, which corresponds to a current VM of the plurality of VMs, is to be utilized to mask access by the current VM to a VMX control word; and

a translation lookaside buffer (TLB) ~~in a processor~~ having a plurality of TLB entries, wherein a ~~each~~ TLB entry of the plurality of TLB entries is to be ~~entry being~~ associated with a virtual machine extension (VMX) tag word, and

invalidation logic to determine the TLB entry is to be invalidated responsive to a comparison of the VMX tag word and the VMX control word indicating the TLB entry is to be invalidated in response to an invalidation operation being performed.

~~indicating if the associated TLB entry is invalidated according to the processor mode when an invalidation operation is performed, the processor mode being one of execution in a virtual machine (VM) and execution not in a virtual machine, the invalidation operation belonging to a non-empty set of invalidation operations composed of a union of (1) a possibly empty set of operations that invalidate a variable number of TLB entries, (2) a possibly empty set of operations that invalidate exactly one TLB entry, (3) a possibly empty set of operations that invalidate the plurality of TLB entries, (4) a possibly empty set of operations that enable and disable use of virtual memory, and (5) a possibly empty set of operations that configure physical address size, page size or other virtual memory system behavior in a manner that changes the manner in which a physical machine interprets the TLB entries[.];~~

~~wherein the invalidation operations include IA-32-specific operations (a) IA-32 task switches involving changes of virtual memory related control registers, or (b) loading of control registers that modify IA-32-specific page size extension (PSE) and physical address extension (PAE).~~

2. (Currently amended) The apparatus of claim 1 wherein the invalidation operation is selected from a group consisting of ~~one of~~ (1) a load~~ing~~ of a first control register conditioned on a global bit, (2) an execution of a page invalidate instruction, (3) ~~an~~ ~~IA-32~~ task switch involving change of at least one virtual memory related control register ~~a task switch that modifies the first control register,~~ (4) a load~~ing~~ of a second control register that modifies one of a protected mode indicator and a page mode indicator, and (5) a loading of a third control register that modifies one of ~~an IA-32 specific~~ page size extension (PSE), a page global enable (PGE), and a physical address extension (PAE).

3. – 10. (Cancelled)

11. (Currently Amended) The apparatus of claim 1 [[10]] further comprising a first register to hold the VMX control word and a second register to hold the current VMX mask word value. ~~wherein the control word or words associated with the TLB are located in one or more of the control registers of the processor or in a Virtual Machine Control Structure (VMCS) in memory~~.

12. (Currently Amended) The apparatus of claim 1 [[11]] further comprising a memory to hold a virtual machine control structure (VMCS), wherein the VMX control word is to be held in the VMCS. ~~wherein one of the control words associated with the TLB is distinguished such that the VMX tag word is set to match a distinguished control word for a new TLB entry, the distinguished control word associated with the TLB being designated the TLBVMX word~~.

13. (Cancelled)

14. (Currently Amended) The apparatus of claim 1 [[13]] wherein the invalidation logic to determine the TLB entry is to be invalidated responsive to a comparison of the VMX tag word and the VMX control word indicating the TLB entry is to be invalidated in response to an invalidation operation being performed comprises: determining the TLB entry is to be invalidated in response to the invalidation operation being performed and the VMX tag word matching the VMX control word. ~~the TLB entry is invalidated when an invalidation operation is performed and the value of the associated VMX tag word matches the value of the TLBVMX word and the processor mode corresponds to execution in a virtual machine (VM)~~.

15. (Currently Amended) The apparatus of claim 1 [[14]] wherein the ~~one or more~~ VMX control word[[s]] ~~associated with the TLB, including the TLBVMX word, are~~ is configurable ~~when the processor mode corresponds to execution not in~~ a non-virtual machine execution mode.

16. – 19. (Cancelled)

20. (Currently Amended) The apparatus of claim 1 [[18]] further comprising a second VMX control word, wherein the invalidation logic is to determine the TLB entry is to be invalidated responsive to ~~when an invalidation operation is performed and the~~ a logical AND of the ~~associated~~ VMX tag word and the second VMX control word ~~associated with the TLB~~ matches the [[TLB]]VMX control word ~~and the processor mode corresponds to execution in a virtual machine, the second control word associated with the TLB being designated the TLBVMX mask word~~.

21. (Currently Amended) The apparatus of claim 20 wherein ~~access by software to configure a portion of the TLBVMX word when the processor mode corresponds to execution in a virtual machine (VM) is conditioned upon value of the TLBVMX mask word such that software executing when the processor mode corresponds to execution in a virtual machine (VM) is able to set the TLBVMX word to a value such that the~~ a logical AND of ~~a new value of~~ the current [[TLB]]VMX mask word and ~~a value of the~~ a previous [[TLB]]VMX mask word matches the previous VMX mask word ~~a logical AND of a previous value of the TLBVMX word and the value of TLBVMX mask word~~.

22. Cancel.

23. Cancel.

24. Cancel.

25. (Currently Amended) The apparatus of claim 1 [[20]] wherein ~~the bits configured in~~ the VMX tag word and the [[TLB]]VMX control word are determined by ~~an~~ execution of a specified processor instruction in a specified manner.

26. Cancel.

27. – 33. (Cancelled)

34. (Currently Amended) The apparatus of claim 1 [[16]] wherein a size of a VMX tag word and the [[TLB]]VMX control word is determined by executing a specified processor instruction in a specified manner.

35. (Currently Amended) The apparatus of claim 34 wherein ~~the processor is compatible with the Intel Architecture and~~ the specified instruction is a central processor unit identification (CPUID) instruction and the specified manner is to have a specified value in a[[n]] control ~~EAX~~ register when the CPUID instruction is executed.

36-70. (Cancelled)

71. (Currently Amended) A processor comprising:

a virtual machine extension (VMX) mask word to mask access to VMX control (TLBVMX) word during a VMX mode of operation;

a translation lookaside buffer (TLB) having a plurality of TLB entries, each TLB entry being associated with a virtual machine extension (VMX) tag word; and

invalidation logic, in response to an invalidation operation during the VMX mode of operation, to invalidate each TLB entry being associated with a VMX tag word that matches the TLBVMX word. ~~indicating if the associated TLB entry is invalidated according to a the processor mode when an invalidation operation is performed , the processor mode being one of execution in a virtual machine (VM) and execution not in a virtual machine, the invalidation operation belonging to a non-empty set of invalidation operations composed of a union of (1) a possibly empty set of operations that invalidate a variable number of TLB entries, (2) a possibly empty set of operations that invalidate exactly one TLB entry, (3) a possibly empty set of operations that invalidate the plurality of TLB entries, (4) a possibly empty set of operations that enable and disable use of virtual memory, and (5) a possibly empty set of operations that configure physical address size, page size or other virtual memory system behavior in a manner that changes the manner in which a physical machine interprets the TLB entries; and~~

~~first, second, and third registers coupled to the TLB to store information related to the invalidation operation;~~

~~wherein the invalidation operations include IA-32 specific operations (a) IA-32 task switches involving changes of virtual memory related control registers, or (b) loading of control registers that modify IA-32 specific page size extension (PSE) and physical address extension (PAE).~~

72. (Currently Amended) The processor of claim 71 wherein the invalidation operation is selected from a group consisting of ~~one of~~ (1) a loading of the first control register conditioned on a global bit, (2) an execution of a page invalidate instruction, (3) ~~an IA-32~~ a task switch involving change of at least one virtual memory related control register, and (5) a loading of the third control register that modifies one of a[[n IA-32-specific]] page size extension (PSE), a page global enable (PGE), and a physical address extension (PAE).

73. (Currently Amended) The processor of claim 71 [[72]] wherein invalidation logic, in response to an invalidation operation during the virtual machine mode of operation, to invalidate each TLB entry being associated with a VMX tag word that matches the TLBVMX word comprises: the invalidation logic, in response to an invalidation operation during the virtual machine mode of operation, to updated each VMX tag word that matches the TLBVMX word to an invalid value to indicate each TLB entry being associated with each VMX tag word that matches the TLBVMX word is invalid. ~~the processor is in or not in VMX mode and the TLB entry is not invalidated at loading of the first control register when one of a transition into VMX mode (a VM entrance) and a transition out of VMX mode (a VM exit) occurs~~.

74. (Currently Amended) The processor of claim 71 [[72]] further comprising a hardware management stack to hold a plurality of mask values for the VMX mask word, wherein each of the plurality of mask values correspond to a layered virtual machine. ~~wherein the VMX tag word is a single bit and the VMX tag word is negated for a new TLB entry when the processor is not in VMX mode and the VMX tag word is asserted for a new TLB entry when the processor is in VMX mode; and the TLB entry is invalidated when an invalidation operation is performed and the VMX tag word is asserted and the processor is in VMX mode.~~

75. (Currently Amended) The processor of claim 71 [[74]] wherein the invalidation logic, in response to an invalidation operation during a non-VMX mode of operation, to invalidate a ~~the~~ TLB entry of the plurality of TLB entries ~~is invalidated~~ irrespective of ~~value of~~ the VMX tag word being associated with the TLB entry ~~when an invalidation operation is performed and the processor is not in VMX mode~~.

76. - 80. (Cancelled)